Design of Integrated Circuit for Differential Variable Capacitors

1. Field of the Invention:

[0001] The present invention relates to an integrated circuit design for differential variable capacitors, more particularly to an integrated circuit being integrated with differential variable capacitors and having no asymmetric coil for reducing the chip size, lowering the circuit inaccuracy, and controlling the overall loading quality of variable capacitors effectively.

2. Background of the Invention:

[0002] A voltage control oscillator (VCO) is an important circuit indispensable to the applications of radio frequency (RF)/microwave and wireless communication, which uses a bias voltage to enable the variable capacitor therein to vary its capacitance, and thus further changes the oscillating frequency.

[0003] More and more people adopt differential circuit design for the circuit of voltage control oscillators (VCO) to reduce the interference caused by common-mode noises. To achieve the differential effect, differential variable capacitors become an essential component. However, the conventional differential variable capacitor usually consists of two independent capacitors, and such arrangement not only increases the chip size, but also enhances a circuitry inaccuracy due to the parasitic effect occurring between the two independent capacitors.

[0004] As seen in FIGS. 1A and 1B, a conventional differential variable capacitor is consisted of a first capacitor 1 and a second capacitor 2. The circuit design of the conventional differential variable capacitor is as following: respectively forming n+ implant points 12, 22 in n-well regions 11, 21 on p-substrates 10, 20; connecting the n+ implant points 12, 22 to form a bias voltage control point Vc; employing P1 and P2 as the contacts for connecting to other circuits; and employing p+ implant points 13, 23 as the grounding point.

[0005] In view of the circuit design of the conventional differential variable capacitor, there exists at least the following shortcomings:

1. The conventional differential variable capacitor adopts two independent capacitors. Therefore, a larger chip is required for the making of the differential variable capacitor such that the manufacturing cost is increased.

2. Parasitic effects will occur at the connection between the two independent variable capacitors of the conventional differential variable capacitor, and thus increasing the circuitry inaccuracy.

3. Since the connection between two variable capacitors must be symmetrical, therefore the positioning has to be very precise, and thus increasing the level of difficulty of the manufacture.

4. Asymmetry usually occurs in the connection between the two variable capacitors, and thus greatly reducing the differential effect.

5. In the conventional differential variable capacitor, there is no way of knowing the factor of overall loading quality of the variable capacitor.

SUMMARY OF THE INVENTION

[0006] In view of the shortcomings of the prior arts, the primary object of the present invention is to provide an integrated circuit design of a differential variable capacitor, using an integrated method to design an integrated circuit of a differential variable capacitor with the consideration of solving the parasitic effect occurred therein so as to reduce the circuitry inaccuracy.

[0007] Another object of the present invention is to provide an integrated circuit design of a differential variable capacitor, using an integrated method to design an integrated circuit of a differential variable capacitor to effectively reduce the chip size and lower the manufacturing cost.

[0008] Yet, another object of the present invention is to provide an integrated circuit design of a differential variable capacitor, using an

integrated method to design an integrated circuit of a differential variable capacitor to prevent the happening of asymmetric coils.

[0009] Yet, another object of the present invention is to provide an integrated circuit design of a differential variable capacitor, capable of knowing the factor of overall loading quality of the variable capacitors, and thus further effectively controlling the overall loading quality of the variable capacitors.

[0010] Yet, another object of the present invention is to provide an integrated circuit design of a differential variable capacitor, which is integrally formed without the need of repositioning for achieving a symmetrical connection, and thus has a very precise positioning so as to reduce the level of difficulty of manufacturing the same.

[0011] To achieve the foregoing objectives, the present invention provides an integrated circuit design of a differential variable capacitor, which comprises: a p-substrate; an n-well region disposed on the top surface of the p-substrate; at least three n-type ion implant regions, each disposed on the top surface of the n-well region; a metal wire for connecting the three n-type ion implant regions; a bias voltage control point, coupled to the n-type ion implant region; a first gate; and a second gate being coupled with the first gate; wherein the first gate and second gate use the bias control point as center to be disposed symmetrically on both sides of the bias voltage control point. Therefore, the integrated circuit uses an integrated design to integrally form the differential variable capacitor, and the parasite effect is also taken into consideration in the manufacturing process for reducing the circuitry inaccuracy, lowering the manufacturing cost, and preventing asymmetric coils from happening. The present invention provides the knowledge about the factor of overall loading quality of the variable capacitors, and thus further effectively controls the overall loading quality of the variable capacitors during manufacturing the same. Furthermore, the present invention does not require repositioning for the symmetric connection, and thus has a very precise positioning so as to reduce the level of difficulty of manufacturing the same.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. 1A is a top view of a conventional differential variable capacitor.

[0013] FIG. 1B is a cross-sectional view of a conventional differential variable capacitor.

[0014] FIG. 2A is a top view of a differential variable capacitor according to a first preferred embodiment of the present invention.

[0015] FIG. 2B is a cross-sectional view of a differential variable capacitor according to a first preferred embodiment of the present invention.

[0016] FIG. 3A is a top view of a differential variable capacitor according to a second preferred embodiment of the present invention.

[0017] FIG. 3B is a cross-sectional view of a differential variable capacitor according to a second preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0018] For your esteemed members of reviewing committee to further understand and recognize the objectives, the characteristics, and the functions of the invention, a detailed description in matching with corresponding drawings are presented as the following.

[0019] Please refer to FIGS. 2A and 2B for the top view and cross-sectional view of a preferred embodiment of the present invention respectively, wherein the integrated circuit of a differential variable capacitor 3 forms an n-well 31, using an ion implant method to implant at least three n-type ion implant regions 32 disposed on the top surface of the n-well. The n-type ion implant regions 32 include a first n-type ion implant region 32a, a second n-type ion implant region 32b, and a third n-type ion implant region 32c; wherein the first n-type ion implant region 32a and the third n-type ion implant region 32c use the second n-type ion implant region 32b as the center to be disposed symmetrically on both sides of the second

n-type ion implant region 32b. Since the relative positions of the first n-type ion implant region 32a, second n-type ion implant region 32b, and third n-type ion implant region 32c can be confirmed in the ion implantation, so that the differential variable capacitor 3 is designed as a whole, which no longer needs to reposition for the symmetric connection.

[0020] The conventional lithographic and etching technologies are used to form a structure using the contact point of an oxide layer to connect the connecting points and metal wire; wherein the metal wire 33 connects the foregoing n-type ion implant region 32b; the first gate 34 is disposed in the metal wire 33 and between the first n-type ion implant region 32a and the second n-type ion implant region 32b; the second gate 35 is also disposed in the metal wire 33 and between the second n-type ion implant region 32b and the third n-type ion implant region 32c; the bias voltage control point 36 is coupled to the first n-type ion implant region 32a, the second n-type ion implant region 32b, and the third n-type ion implant region 32c; the first contact point 37 is coupled to the first gate 34; the second connecting point 38 is coupled to the second gate 35, wherein the first connecting point 37 and the second connecting point 38 use the bias voltage control point 36 as the center to be disposed symmetrically on both sides of the bias voltage control point 36.

[0021] Since the differential variable capacitor 3 is designed as a whole, therefore asymmetric coils will not occur, and we can know about the factor of overall loading quality of the variable capacitor to effectively control the overall loading quality of the variable capacitor. Further, the p-substrate at its top surface further comprises a p-type ion implant region 39 coupled to a grounding point 40 for the purpose of grounding. The first gate 34 and the second gate 35 according to a preferred embodiment of the present invention is made of a poly-silicon material.

[0022] Please refer to FIGS. 3A and 3B for the top view and the cross-sectional view according to a second preferred embodiment of this invention respectively, wherein the integrated circuit of the differential variable capacity 5 forms a p-well 51 at the top surface of a n-type substrate 50 and uses at least three p-type ion implant regions 52 disposed on the top surface

of the p-well 51. The three p-type ion implant regions 52 include a first p-type ion implant region 52a, a second p-type ion implant region 52b, and a third p-type ion implant region 52c, wherein the first p-type ion implant region 52a and the third p-type ion implant region 52c use the second p-type ion implant region 52b as the center to be disposed symmetrically on both sides of the second p-type ion implant region 52b. Since the positions of the first p-type ion implant region 52a, the second p-type ion implant region 52b, and the third p-type ion implant region 52c are confirmed during the ion implantation, so that the differential variable capacitor 5 is designed as a whole, and does not require repositioning for the symmetrical connection at a later manufacturing process.

[0023] The conventional lithographic and etching technologies are used to form a structure using the contact point of an oxide layer to connect the connecting points and metal wire; wherein the metal wire 53 connects the foregoing at least three p-type ion implant points 52; the first gate 54 is disposed in the metal wire 53 and between the first p-type ion implant region 52a and the second p-type ion implant region 52b; the second gate 55 is also disposed in the metal wire 53 and between the second p-type ion implant region 52b and the third p-type ion implant region 52c. The bias voltage control point 56 is coupled to the first p-type ion implant region 52a, the second p-type ion implant region 52b, and the third p-type ion implant region 52c; the first connecting point 57 is coupled to the first gate 54; the second connecting point 58 is coupled to the second gate 55, wherein the first connecting point 57 and the second connecting point 58 use the bias voltage control point 56 as the center to be disposed symmetrically on both sides of the bias voltage control point 56, which are also the first gate 54 and the second gate 55 and use the bias voltage control point 56 as the center to be disposed symmetrically on both sides of the bias voltage control point 56.

[0024] Further, the n-type substrate 50 at its top surface comprises an n-type ion implant region 59 coupled to a grounding point 60 for the purpose of grounding. The differential variable capacitor 5 is also designed as a whole, which has the same effect as the first preferred embodiment, and thus will not be described here.

[0025] In view of the description above, the present invention discloses an integrated circuit design of a differential variable capacitor, which is applicable for both the n-type semiconductor substrate and the p-type semiconductor substrate. The present invention uses an integrated method to design an integrated circuit of the differential variable capacitor to effectively reduce the chip size and lower the manufacturing cost. The present invention can prevent asymmetrical coils, and allows us to know about the factor of overall loading quality of the variable capacitor, and further effectively control the overall loading quality of the variable capacitor.